

10
FOR (i=0; i<2; i=i+1)
11 { begin
out [i] = 8 ' b10101010;
enable [i] = up [2 * i];
end }

Figure 1

(Prior Art)

13
reg y [3:0];
12 WHILE (x <= y)
begin
fpl_bit [x + y] - mm_iru [x - y];
end

Figure 2

(Prior Art)

16 18 20 14 22
FOR (INIT; EXIT; INC)
begin
BODY_OF_STATEMENTS;
end

Figure 3

(Prior Art)

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```
out [ 0 ] = 8 ' b10101010 ;  
enable [ 0 ] = ~up [ 0 ] ;  
  
out [ 0 ] = 8 ' b10101010 ;  
enable [ 0 ] = ~up [ 2 ] ;
```

} 24

Figure 4

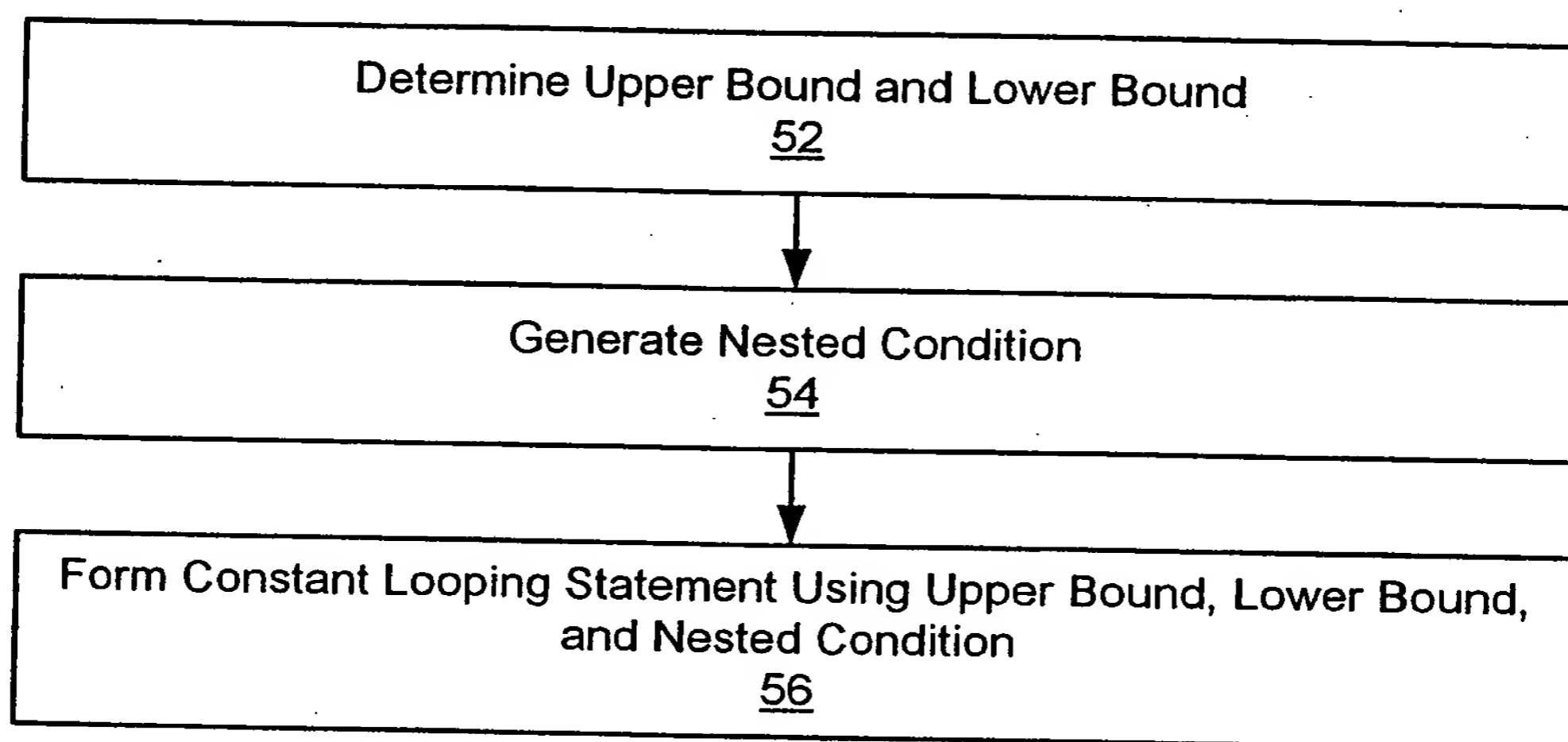


Figure 5

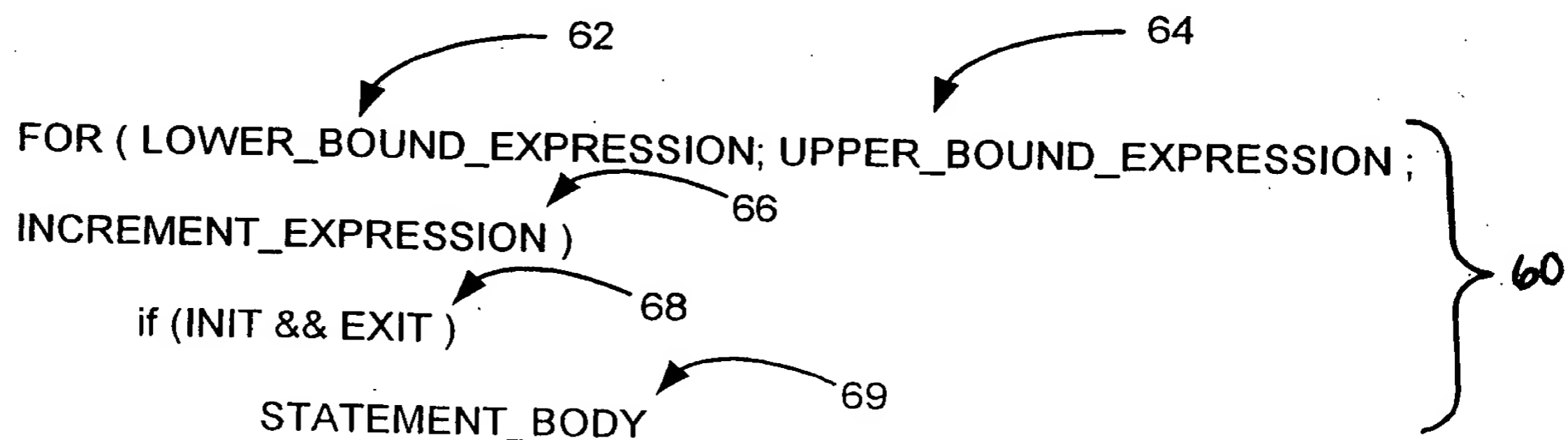


Figure 6